UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/078,690	02/19/2002	David A. Petersen	2001P20913US	6224

7590 05/14/2004

Siemens Corporation
Intellectual Property Department
186 Wood Avenue South
Iselin, NJ 08830

EXAMINER	
JAWORSKI, FRANCIS J	
ART UNIT	**PAPER NUMBER**
3737	8

DATE MAILED: 05/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/078,690	Applicant(s) PETERSEN ET AL.	
	Examiner Jaworski Francis J.	Art Unit 3737	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39 are* is/are pending in the application.

4a) Of the above claim(s) *22-39 are* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 June 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1.5*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The substitute specification filed 09-03-02 has been entered.

Claims 22-39 stand withdrawn from consideration at this time, having been non-elected without traverse in paper .No. 7.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(Parenthesized claim numbers where present indicate the specific claim or claims towards which the Examiner's immediately preceding argument is directed.)

Claims 1-2 are rejected under 35 U.S.C. 102(b) as being anticipated by Bates (US3768000). Bates teaches an implementation method for producing a multi-level transmit waveform Eo of Fig.5 and leads 8, 10 of Figure 4, wherein transistors and other switch devices serve to alter voltage levels to the transformer series secondary 4, 4', see col. 2 lines 33-37. (The Examiner is interpreting 'transmit' as meaning 'output' rather than any narrower construal in the wave propagation sense. For example Bates' Eo might be expected to be 'transmitted' or supplied to a line or cable.). (Claim 1).

Bates applies first voltages Ea, Eb and second voltages Ea', Eb' to respective series transformers 4, 4', and additionally supplies turn-off voltage segments Er, Er' thereto. (Claim 2).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3 - 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bates (US3768000) in view of Dhyanchand et al (US5177460). Bates is applied as discussed above. Bates does not specifically teach the establishment of separate flux paths since it does not treat the specific core geometry of the output transformer(s). However since it was well-known in the transformer art to link a single output winding to plural inputs via separate flux paths as taught in Dhyanchand et al Figs. 5-6 and attendant discussion, it would have been obvious to incorporate same into Bates for purposes of space and power transfer efficiency under this general design principle since both are concerned with production of stepped sinusoid outputs. (Claim 3).

The sub-inverters of Dhyanchand '460 and/or the transistor switches of Bates serve to superpose signals onto the windings of the flux core.including up to four such signals in consideration of the aforementioned Bates contributiong voltages. (Claims 4-5, 7).

In simplest form the stepped waveform AC of Dhyanchand et al col. 1 or Eo of Bates Fig. 5 would reduce to +1, 0, -1 levels. or simple alternating pulse inversion. (Claim 6).

In Bates, transistor switches S1 and S2 connected to opposite ends of first primary winding 4a,b may be functionally 'closed'. (Claim 8).

In Bates, either end of winding 4a,4b may be grounded via tie common node 12e. (Claim 9).

Voltage sources for example Ea, Ea' in Bates are of differing amplitudes and when applied to respective primary windings 4a,4b, 4a',4b'. (Claim 10).

In order to produce the Bates output the application voltages variously sum and subtract through the stepped waveform cycle and include zero levels in order that transformer core saturation be avoided, see col. 5 lines 42-53. (Claims 11-12).

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bates in view of Dhyanchand et al as applied to claim 4 above, and further in view of Piechnick (US4996637). Whereas the Bates-Dhyandchand et al combination would not specifically teach the production of at least eight non-zero voltage levels, it would have been obvious in view of Piechnick Fig. 8, 9 and Fig. 10D that a switched (in this case thyristor latch switches) series primary winding set used to produced a stepped output waveform as in the former may be used to produce a relatively high number of voltage levels simply by organizing the switching controls into repeating stages. (Claim 13).

Claims 14 – 19 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bates as applied to claim 2 above, and further in view of Hayashi et al (US6724607) and Oppelt et al (US6083164, of record). It would have been obvious in view of the latter to provide a positive-negative cycle AC output such as might be derived from a D.C. source by a switching inverter circuit providing the stepped

sinusoid as an AC approximation as in Bates to piezoelectric actuators 12-15 of Hayashi et al since the latter is referring to imaging transducers, see col. 1 lines 7-10, and Oppelt et al merely serves as a reference of convenience to evidence that such transducers are in fact ultrasound transducers. (Claims 14, 19).

The primary winding 4a,4b in Bates is tapped by three voltage sources, Ea, Eb and either or both of Ea', Eb' fed via switch 14' to the 4a,4b centertap and with action of switches S1,S2, 14, 14' including grounding of the switches as discussed above. (Claim 15).

In order that a stepped sinusoid be produced in Bates (for purposes of providing AC drive to an ultrasound imaging device such as Hayashi et al v Oppelt et al) the contributory voltages E1 and E2 derived from first and second transformers 4 and 4' must differ in peak pulse magnitude, whereupon it would have been inherently obvious to a circuit designer to alter the winding ratio of 4c with respect to 4c'. (Claim 16).

When switches S1 and S2 respectively operate the primary windings 4a, 4b and 4a', 4b' connect to the same voltage node, i.e. the Ea-Eb common node. (claim 17).

The number of states of the first or E1 voltage and the second or E2 voltage differ per unit time, again see Fig. 5 which depicts behavior along a unified time base. .(Claim 18).

With respect to claim 21, see discussion of Dhyandchand et al '460 against claims 4-5,7 supra. (Claim 21).

Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bates in view of Hayashi et al as applied to claim14 above, and further in view of Dhyanchand et al '460 as the latter was applied above to evidence how the transformer designer might arrange a separate flux path geometry in order to implement a voltage-summing/subtracting transformer output stage. (Claim 20).

Bates (US3579081) is cited as of interest insofar as it forms the backdrop for the Bates improvement patent used in the rejections, see col. 1 lines 28-53 of the latter.

Miller (US4032832) is cited for figs. 1-2 and 5 and is of the Genre of the Bates patents.

Dyanchand et al (US5027265) is cited for its Fig. 4a and as related technology to the '460 patent.

Any inquiry concerning this communication should be directed to Jaworski Francis J. at telephone number 703-308-3061.

Francis J. Jaworski
Primary Examiner

FJJ:fjj

05-01-04